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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 002282.P066 Total Pages 2

First Named Inventor or Application Identifier Roberto Suaya

Express Mail Label No. EL034433195US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 23)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 8)

4. X Oath or Declaration (Total Pages 4)

a. xx Unsigned

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. __ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. xx Other: Certificate of Mailing (1 page in duplicate)

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

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18. **Correspondence Address**

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or

X Correspondence Address Below

NAME Paul A. Mendonsa, Reg. No. 42,879

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (503) 684-6200 FAX (503) 684-3245

Express Mail Label: EL034433195US

Title: **CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT**
Inventor(s): Suaya et al.
Our Reference: 002282.P066

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Paul A. Mendonsa — Aug 26, 1999
Paul A. Mendonsa — Date:
Reg. No. 42,879

"Express Mail" mailing label number: EL034433195US
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Serial/Patent No.: ********** Filing/Issue Date: August 26, 1999
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Title: CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT

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Date Mailed: Auguest 26, 1999 Docket Due Date: n/a

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- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
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- ☐ Application - Rule 1.53(b) CIP (____ pgs.)
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UNITED STATES PATENT APPLICATION

FOR

CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT

INVENTORS:

ROBERTO SUAYA
SOPHIE GABILLET

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(503) 684-6200

CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The invention relates to circuit design parameter measurement. More particularly, the invention relates to a method and apparatus for high precision measurement of cross coupling and total capacitance of wires on an integrated circuit design.

BACKGROUND OF THE INVENTION

Until the advent of deep sub micron integrated circuit processes, timing behavior of integrated circuits has been dictated by transistor considerations, mostly transistor travel time and the number of logic levels a signal traverses during a clock cycle. Accurate models of transistor device parameters were the key element for the prediction of circuit timing behavior.

For feature sizes larger than 0.35 μm wire delay is typically less than 20% of total timing delay. To account for the 20% contribution to total timing delay high precision delay estimates were not required for wire delay. A relatively large (e.g., 25%) uncertainty in extracting resistance and/or capacitance values results in approximately a 4% overall error in time delay modeling.

Computer aided design (CAD) programs used for integrated circuit design used simplified models to compute wire delay from resistance and capacitance data extracted using a layout database. Resistance and capacitance models that provide less than 25% uncertainty are well known in the art. For example, resistance estimates can be generated based on the geometric shape of the line to be estimated. Capacitance estimates can be

generated based on a parallel plate capacitor model with perimeter fringe contribution corrections. These modeling approaches are useful for integrated circuit designs having device sizes greater than 0.35 μm.

However, as device sizes decrease the relative importance of wire delay increases. Wire extraction programs can be calibrated with accurate measurements of capacitance. One approach to accurate wire capacitance measurement is provided by B.W. McGaughy, J.C. Chen, D. Sylvester and C. Hu "A Simple Method for On-Chip Sub-Femto Farad Interconnect Capacitance Measurement," IEEE Electron. Device Letters, Vol. 18, No. 1, pp. 21-23, January 1997, (hereinafter referred to as "the IEEE paper"), which discloses a method for determining cross coupling capacitance. However, the method described in the IEEE paper suffers shortcomings that are explained in detail in a white paper by J. C. Chen and Roberto Suaya entitled "Proper On-Chip Capacitance Measurement," (hereinafter referred to as "the white paper"). A brief overview of the white paper is provided below.

Figure 1 represents the circuit used in the IEEE paper to measure cross coupling capacitance. A general method to measure capacitance consists of measuring the total charge deposited on the capacitor, which can be accomplished by measuring DC currents, frequency of applied signals, and voltage. The following formula permits the determination of capacitance:

$$I = CV_{dd}f \qquad \text{(Equation 1)}$$

where I is a dc current reading, C is a load capacitance, V_{dd} is the voltage supply level, and f is the frequency of the waveforms applied.

The voltage waveform of **Figure 2** used in the IEEE paper are non-overlapping waveforms that provide, except for leakage, no current path between V_{dd} and ground in the circuit of Figure 1. In the IEEE paper, the unknown capacitance is measured as the difference between two current readings on the two current meters in Figure 1. The process is flawed because of charge redistribution. The capacitance coupling between two structures, depends on the presence of other nearby structures.

Consider in Figure 1, two identical load structures, C and C'. The capacitance of C to ground on the left side of the structure is different from the capacitance C' to ground on the right side. The difference is due to the redistribution of the electric field due to the presence of the second conductor. The capacitance difference can be quite large.

Configurations like the one shown in **Figure 3**, where the load wire and its neighbors are on the same physical layer and are separated by minimum distance, constitute a case where the direct application of the method of the IEEE paper would result in up to 70% error in the extraction of the unknown cross coupling capacitance. There is, in addition, the uncertainty related to the lack of equality in the capacitance of the transistors on the two sides of the mirror structure. This additional source of error becomes more significant as the device size decreases.

SUMMARY OF THE INVENTION

A method and apparatus for determining cross coupling capacitance of wires in an integrated circuit. A first predetermined signal is applied to a first wire. A second predetermined signal is applied to a second wire that is parallel to the first wire. A cross coupling capacitance between the first wire and the second wire is determined based, at least in part, on a current signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example, and not by way of limitation in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a prior art circuit for use in measuring cross coupling capacitance.

Figure 2 is a voltage waveform for use to measure the capacitance of the circuit of Figure 1.

Figure 3 is a prior art circuit for measuring cross coupling capacitance between parallel wires on the same layer that leads to large errors.

Figure 4 is a circuit suitable for use in determining cross coupling capacitance according to one embodiment of the invention.

Figure 5 is a voltage waveform for use in measuring the cross coupling capacitance of the circuit of Figure 4 according to one embodiment of the invention.

Figure 6 is an equivalent circuit diagram corresponding to the circuit of Figure 4.

Figure 7 is one among the multiple extensions of the measuring device method shown in Figure 4 to multiple wire configurations.

Figure 8 is a block diagram illustrating an overview of an IC design simulation tool.

Figure 9 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention.

Figure 10 is one embodiment of a computer system suitable for use with the invention.

DETAILED DESCRIPTION

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

The invention provides a method and apparatus for determining cross coupling capacitance of wires in an integrated circuit, total capacitance can be determined by adding the different cross coupling capacitance. The capacitance information derived according to the invention can be used, for example, to calibrate a parasitic extraction engine or to calibrate an integrated circuit fabrication process. The capacitance information can also be used to improve timing and noise simulations of circuits particularly for deep sub-micron circuits since wire capacitance effects play a dominant role for deep submicron circuits.

Briefly, the invention allows the measurement of cross coupling capacitance between two lines by applying predetermined voltage signals to specific circuit elements. The resulting current allows for simple computation of cross coupling capacitance, and

total capacitance by addition. The capacitance values obtained can then be used to calibrate extraction engines, processes, and provide input to timing and noise simulators.

Figure 4 is a circuit suitable for use in determining cross coupling capacitance according to one embodiment of the invention. The circuit of Figure 4 removes transistor mismatch and charge redistribution errors, which improves the accuracy of measurement as compared to Figures 1 and 3 above.

The main structure of Figure 4 includes ammeter 400, transistor 410, transistor 420 and a minimum size structure that connects load wire 440 with the main structure. In the example of Figure 4, load wire 440 and neighbor wire 450 are on the Metal2 layer; however, Metal2 layer wires are not required. In the embodiment of Figure 4, load wire 440 is coupled to the main structure by Metal1-via-Metal2 structure 435 and wire 430.

The circuit of Figure 4 is used to measure cross coupling capacitance between wire 440 and wire 450, Wire 440 is parallel to wire 450. Inverter 460 is coupled to wire 450 by wire 455. In one embodiment, inverter 460 is far enough away from the main structure to reduce noise input on wire 400.

Figure 5 is a voltage waveform for use in measuring the cross coupling capacitance of the circuit of Figure 4 according to one embodiment of the invention. Voltage V_1 is applied to the gate of transistor 420. Voltage V_2 is applied to the gate of transistor 410. Voltage V_3 is input to inverter 460. Referring back to Figure 4, only the portion of the line (i.e., wire 450 and 455) driven by V_3 (i.e., wire 450) gives an appreciable contribution to the cross coupling capacitance affecting line segment 440. Capacitance measuring for the circuit of Figure 4 using the voltage waveforms of Figure 5 are described below.

Figure 6 is an equivalent circuit diagram corresponding to the circuit of Figure 4. With reference to the circuit of Figure 6, the following name convention applies: C_1, C_2, C_{line}, and $C_{coupling}$ refer, respectively, to transistor plus Metal1-via-Metal2 minimum structure and other parasitic capacitances to ground, Metal2 ground capacitance, total capacitance of nearest neighbor, and the capacitance coupling between wires 440 and 450.

Before applying the voltage waveforms of Figure 5, the voltage applied to the external inverter 460, $V_3 = V_{dd}$, (or ground). Ammeter 400 is used to measure the charge, Q, that flows into node 600 of Figure 6. Node 600 gets charged when $V_2 = V_1 = 0$, and this charge is equal to:

$$Q = I / f = (C_1 + C_2 + C_{coupling})V_{dd} \qquad \text{(Equation 2)}$$

The measurement proceeds by applying for a sufficiently large number of cycles a periodic signal to V_3, having the same frequency as the signal applied to V_1, V_2. The relative rise and fall times of the external signals do not matter.

Following the discharge to ground of transistor 420, V_3 is switched to ground, and $C_{coupling}$ is charged to V_{dd}. This charge redistributes among the capacitors because node 600 is in a high impedance state. The intermediate voltage at node 600 is not important, provided that the switching of transistors 420 and 410 is not altered. Next, V_2 is switched to ground and

$$Q' = (C_1 + C_2)V_{dd} \qquad \text{(Equation 3)}$$

flows into node 600. The difference between the direct current readings represented by Equations 2 and 3, (when $V_3 = V_{dd}$, on static mode, and when $V_3 = 0$ on periodic mode) normalized to V_{dd} identifies $C_{coupling}$.

$$C_{coupling} = (Q - Q')/V_{dd} \qquad \text{(Equation 4)}$$

The measurement of $C_{coupling}$ in the circuit of Figure 4 (represented by an equivalent circuit in Figure 6) is free of transistor capacitance influence and insensitive to charge redistribution errors, as compared to the dual mirror structured circuits described in the IEEE paper. However, errors due to a minimum size probe reaching the Metal2 configuration and errors arising from coupling to the orthogonal portion of the aggressor wire to the wire under test remain. In one embodiment, for a 0.25 μm process with SiO dielectric, the error bound is 0.02 fF. The magnitude of this error decreases with scaling and lower permitivity dielectric materials. Thus, the measurement described with respect to Figures 4-6 allows highly accurate measurement of cross coupling capacitance.

In an alternative embodiment, ammeter 400 can be placed between the source of transistor 420 and ground. This alternative embodiment provides the same accuracy and the embodiments described with respect to Figures 4-6.

The measurement technique described with respect to Figures 4-6 is based on static charge measurement. To the extent that the dielectric constant of the medium is frequency independent, the total deposited charge is frequency independent. Statistical error can be made negligible by performing multiple charge measurements at the same and different frequencies, or alternatively, measuring the slope of the charge as a function

of V_{dd}. Both techniques provide a $\sqrt{n}$ improvement in the statistical error, where n is the number of measurements.

The technique of the invention provides improved calibration of several capacitance elements with a single structure because the technique is extensible to simultaneous and non simultaneous switching of multiple neighbors. The timing scheme is similar to the single wire case, with the addition of another voltage signal V_4 feeding via another inverter the second neighbor wire. There are two choices for the timing of V_4: 1) $V_3 = V_4$, the simultaneous switching of the two wires (in this case, the two neighbor wires are identical, and $2C_{coupling}$ is determined thereby halving the absolute error on $C_{coupling}$); or 2)the central wire to the two neighbor wires are determined independently with the same library element, thereby saving valuable space on the silicon chip (V_4 has the same sequencing as V_3, except that $V_4 = V_{dd}$ while V_3 is periodic).

The neighbors can be on different metal layers. For example, a general nearest neighbor configuration can consist of nine wires on three metal layers, where, with one library element one can measure all the couplings from the middle wire in the middle layer to each of its neighbors. There are eight couplings that can be measured with one library element via a direct extension of the last procedure. The overall configuration consists of two V_{dd} lines, one common ground line, two voltages feeding, the N and P transistors of the measuring device and eight voltages feeding the eight nearest neighbor wires. The reason for two V_{dd} lines is to separate the V_{dd} for the measuring structure from the V_{dd} feeding the eight inverters, to reduce noise.

This last technique is particularly useful for library validation. Library validation is the process of building sufficient structures to be measured within the same integrated

circuit chip to characterize a design. Typically, these libraries can be large but kept reasonably small with non simultaneous switching, as described above. The technique of the invention can also be used to optimize process parameters based on wire timing considerations.

Figure 8 is a block diagram illustrating an overview of an IC design simulation tool. As illustrated, IC design simulation tool 800 is constituted with design reader 802, static partitioner 803 and simulation engine 804 comprising dynamic partitioner 807, scheduler 809, node evaluator 808 and model evaluators 806. The elements are operatively coupled to each other as shown. Design reader 802 and some model evaluators 806, in particular a transistor model evaluator and a wire model evaluator, are incorporated with the teachings of the present invention. Certain aspects of static partitioner 803, dynamic partitioner 807 and scheduler 809 are the subject of co-pending U.S. Patent application number 09/333,124, filed June 14, 1999, and entitled "CIRCUIT SIMULATION USING DYNAMIC PARTITION AND ON-DEMAND EVALUATION" which is hereby fully incorporated by reference.

In one embodiment, the model evaluators evaluate transistor models and wire models having capacitance determined as described above. The capacitance information, both cross-coupling capacitance and total capacitance, can be combined with other device modeling information to provide accurate models and evaluations of the models.

Design reader 802 is used to read design description 810 provided by a designer. Design description 810 includes connectivity information connecting various models modeling electronic devices in the IC design. In one embodiment, in addition to flattening a hierarchical design, design reader 802, also assigns device characterizations

to selected ones of the electronic devices of the IC design. In one embodiment the device characterizations are determined as described above. Static partitioner 803 pre-compiles or pre-partitions the IC design into static partitions as well as pre-processes the static partitions into a form particularly suitable for the dynamic partitioner 807.

During simulation, dynamic partitioner 807 further forms and re-forms dynamic partitions of the IC design that are relevant, referencing the pre-formed static partitions. Scheduler 809 determines whether evaluations are necessary for the dynamic partitions for the particular simulation time step, and schedules the dynamic partitions for evaluation on an as-needed or on-demand basis. Accordingly, node evaluator 808 and model evaluators 806 are selectively invoked on an as needed or on-demand basis to evaluate the states of the connections connecting the models, and various parameter values of the models, such as current, voltage and so forth, respectively.

In one embodiment, at least one of the model evaluators adaptively performs the model evaluations at different accuracy or performance levels in accordance with the assigned device characterizations of the devices. Where accuracy is needed, the evaluations are performed through matrix solution. Formation of static partitions, and formation of dynamic partitions as well as scheduling evaluations on demand, i.e. on an as needed basis are explained in the above identified incorporated by reference co-pending U.S. patent applications. Further detail with respect to circuit simulation is provided in and co-pending U.S. Patent application number 09/333,122, filed June 14, 1999, and entitled "ADAPTIVE INTEGRATED CIRCUIT DESIGN SIMULATION TRANSISOR MODELING AND EVALUATION," which is hereby incorporated by reference.

Figure 9 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention. As illustrated, the present invention includes parasitic extraction tool (PEX) 902 and parasitic database (PDB) 904. PEX 902 generates electrical modeling data for layout nets of an IC design, e.g. a deep sub-micron IC design, and stores the generated electrical modeling data in PDB 904 for use by client applications, such as post layout analysis applications 918. Examples of post-layout analysis applications 918 include Delay Calculator by Ultima Technology of Sunnyvale, CA, and Path Mill and Time Mill by Synopsis Inc. of Mountain View, CA.

PEX 902 generates the electrical modeling data for the layout nets using extracted connectivity and geometrical data of the layout nets. In one embodiment PEX 902 generates capacitive modeling data as described above. As shown, PEX 902 includes read function 906 that operates to input these connectivity and geometrical data of the layout nets. For the illustrated embodiment, the extracted connectivity and geometrical data of the layout nets are input from filtered databases (FDB) 916.

The extracted connectivity and geometrical data are stored in FDB 916 by layout cell hierarchies, one FDB per layout cell hierarchy, and indexed by layout nets. The connectivity and geometrical data were extracted at least in part in accordance with specified parasitic effect windows of the various layers of the IC design. Read function 906 operates to retrieve the connectivity and geometrical data of the layout nets from FDB 916 using the stored layout net indices. FDB 916 is the subject of co-pending U.S. Patent application number 09/052,895, filed March 31, 1998, and entitled "METHOD AND APPARATUS FOR EXTRACTING AND STORING CONNECTIVITY AND GEOMETRICAL DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT

DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference.

PDB 904 is designed to accommodate a large volume of electrical modeling data and concurrent accesses by multiple client applications, which is typically of today's and future deep sub-micron IC designs and design environments. For the illustrated embodiment, PDB 904 has physical organization 914 that allows a large volume of electrical modeling data to be stored in multiple physical media, and application interface 910 that shields physical organization 914 from PDB users, e.g. PEX 902 and post layout analysis applications 918. Additionally, PDB 902 has logical organization 912 that abstracts physical organization 914 to facilitate implementation of application interface 910.

For the illustrated embodiment, PEX 902 includes write function 908 that operates to store the generated electrical modeling data of the layout nets into PDB 904 using application interface 910. In alternate embodiments, write function 908 may store the generated electrical modeling data of the layout nets using either logical and/or physical organizations 912-914. Similarly, selected ones of the client applications, e.g. post-layout analysis applications 918, may also elect to access PDB 904 through logical and/or physical organizations 912-914.

Read function 906 and write function 908 are the subject of co-pending U.S. Patent application number 09/052,915, filed March 31, 1998 and entitled "METHOD AND APARATUS FOR GENERATING AND MAINTAINING ELECTRICAL MODELING DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-

pending application is hereby fully incorporated by reference. Except for read function 906 and write function 908, PEX 902 is intended to represent a broad category of electrical modeling tools known in the art. Examples of these electrical modeling tools include but not limited to Pattern Engine of xCalibre by Mentor Graphics, Columbus by Frequency Technology of San Jose, CA, and Arcadia by Synopsis.

Figure 10 is one embodiment of a computer system suitable for use with the invention. Computer system 1000 can be used, for example, for extraction and/or modeling of integrated circuits using the teachings of the present invention. Computer system 1000 includes bus 1001 or other communication device to communicate information and processor 1002 coupled to bus 1001 to process information. While computer system 1000 is illustrated with a single processor, computer system 100 can include multiple processors and/or co-processors. Computer system 1000 further includes random access memory (RAM) or other dynamic storage device 1004 (referred to as main memory), coupled to bus 1001 to store information and instructions to be executed by processor 1002. Main memory 1004 also can be used to store temporary variables or other intermediate information during execution of instructions by processor 1002.

Computer system 1000 also includes read only memory (ROM) and/or other static storage device 1006 coupled to bus 1001 to store static information and instructions for processor 1002. Data storage device 1007 is coupled to bus 1001 to store information and instructions. Data storage device 1007 such as a magnetic disk or optical disc and corresponding drive can be coupled to computer system 1000.

Computer system 100 can also be coupled via bus 1001 to display device 1021, such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to

a computer user. Alphanumeric input device 1022, including alphanumeric and other keys, is typically coupled to bus 1001 to communicate information and command selections to processor 1002. Another type of user input device is cursor control 1023, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 1002 and to control cursor movement on display 1021.

According to one embodiment, extraction and/or modeling can be performed by computer system 1000 in response to processor 1002 executing sequences of instructions contained in main memory 1004. Instructions are provided to main memory 1004 from a storage device, such as magnetic disk, a read-only memory (ROM) integrated circuit (IC), CD-ROM, DVD, via a remote connection (e.g., over a network), etc. In alternative embodiments, hard-wired circuitry can be used in place of or in combination with software instructions to implement the present invention. Thus, the present invention is not limited to any specific combination of hardware circuitry and software instructions.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof (the measurement of a Metal2 wire capacitance coupling to another Metal2 wire). It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising:

applying a first predetermined signal to a first wire;

applying a second predetermined signal to a second wire, wherein the second wire is parallel to the first wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

2. The method of claim 1 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

3. The method of claim 1 wherein applying a first predetermined signal to the first wire further comprises:

applying a first periodic voltage to a first transistor; and

applying a second periodic voltage to the first wire via an inverter.

4. The method of claim 3 wherein the current signal corresponds to current flowing through the first transistor.

5. A machine readable storage medium having stored therein a plurality of machine executable instructions that implement a parasitic extraction tool that operates to generate electrical modeling data for an integrated circuit (IC) design, wherein the parasitic extraction tool includes a database of capacitance values, wherein the capacitance values are determined by:

evaluating a first predetermined signal on a first wire;

evaluating a second predetermined signal on a second wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

6. The machine readable medium of claim 5 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

7. The machine readable medium of claim 5 further comprising determining, based at least in part on the current signal, a total capacitance of the first wire.

8. The machine readable medium of claim 5 wherein a first predetermined signal on the first wire comprises:

evaluating a first periodic current voltage to the first wire via a transistor; and

evaluating a second periodic current voltage to the first wire via an inverter.

9. The machine readable medium of claim 8 wherein the current signal corresponds to current flowing through the transistor.

10. A machine readable storage medium having stored therein a plurality of machine executable instructions that implement an integrated circuit (IC) design simulation tool, wherein the IC design tool simulates an IC design based on capacitance values determined by:

evaluating a first predetermined signal on a first wire;

evaluating a second predetermined signal on a second wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

11. The machine readable medium of claim 10 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

12. The machine readable medium of claim 10 further comprising determining, based at least in part on the current signal, a total capacitance of the first wire.

13. The machine readable medium of claim 10 wherein a first predetermined signal on the first wire comprises:

evaluating a first periodic current voltage to the first wire via a transistor; and

evaluating a second periodic current voltage to the first wire via an inverter.

14. The machine readable medium of claim 13 wherein the current signal corresponds to current flowing through the transistor.

ABSTRACT

A method and apparatus for determining capacitance of wires in an integrated circuit is described. The capacitance information derived according to the invention can be used, for example, to calibrate a parasitic extraction engine or to calibrate an integrated circuit fabrication process. The capacitance information can also be used for timing and noise circuit simulations, particularly for deep sub-micron circuit design simulations. Briefly, the invention allows measurement of both total capacitance of a line and cross coupling capacitance between two lines by applying predetermined voltage signals to specific circuit elements. The resulting current allows simple computation of total capacitance and cross coupling capacitance. Multiple cross coupling capacitance can be measured with a single device, thus improving the art of library generation, and the overall method is free of uncertainties related to transistor capacitance couplings. The capacitance values obtained can then be used to calibrate procedures, processes, devices, etc.

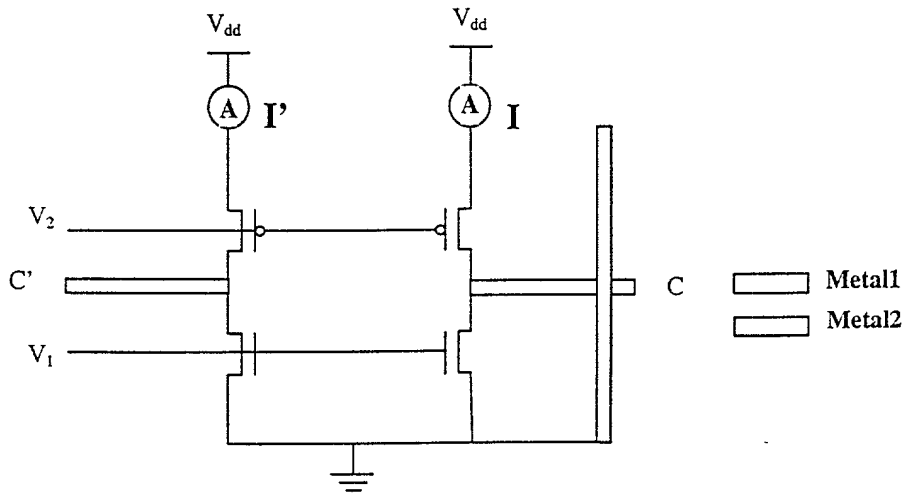

FIG. 1

(PRIOR ART)

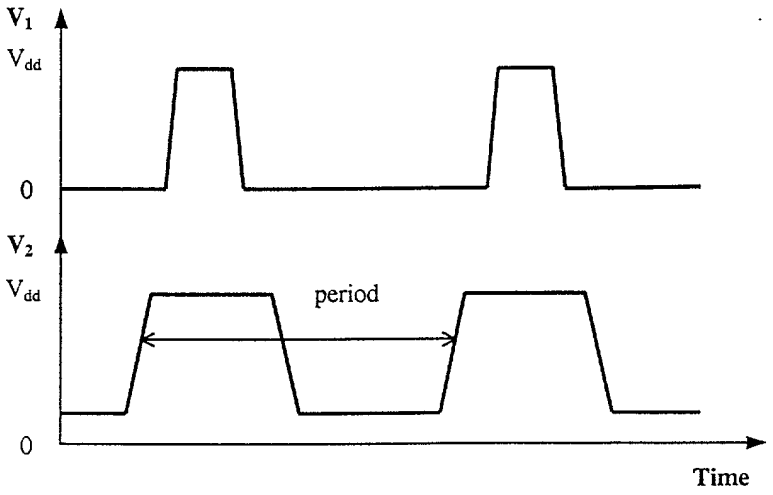

FIG. 2

(PRIOR ART)

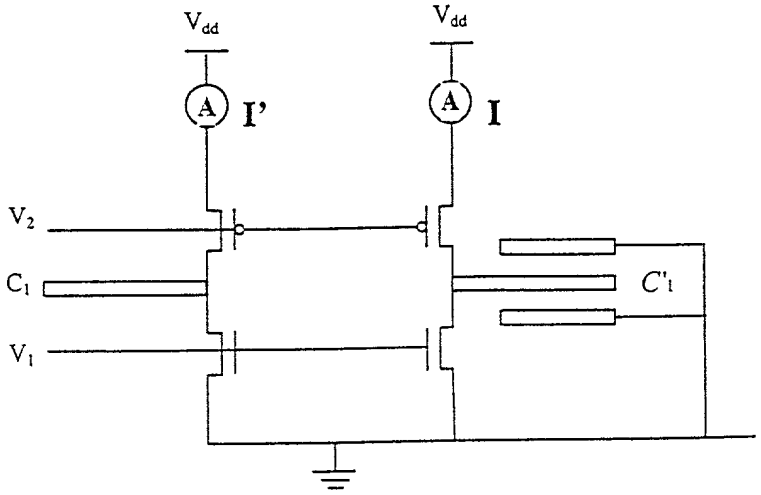

FIG. 3 (PRIOR ART)

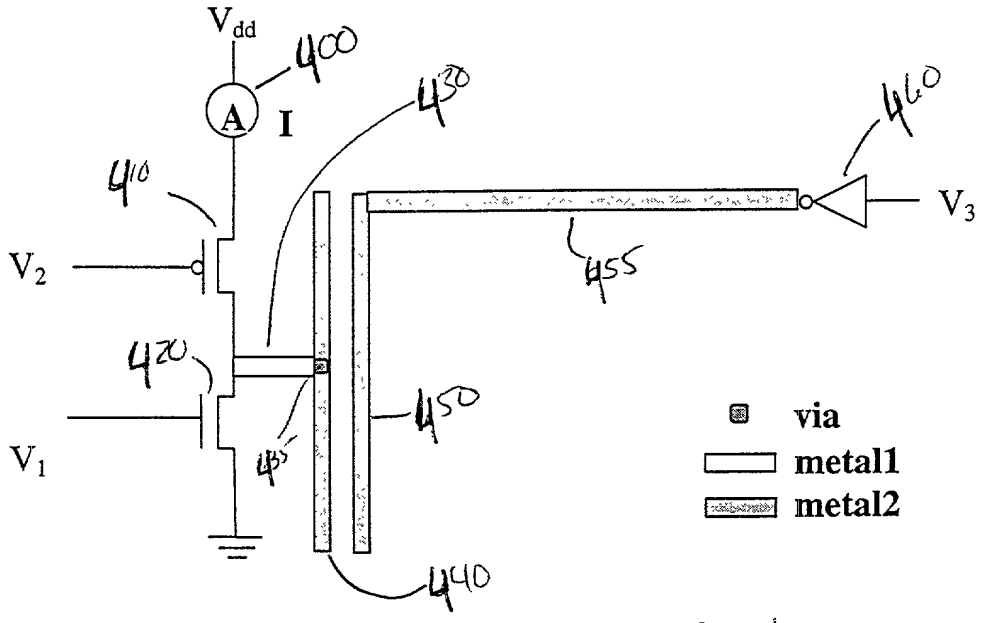
V_{dd}
400
A
I
410
430
460
V_3
455
V_2
420
450
V_1
435
via
metal1
metal2
440

FIG. 4

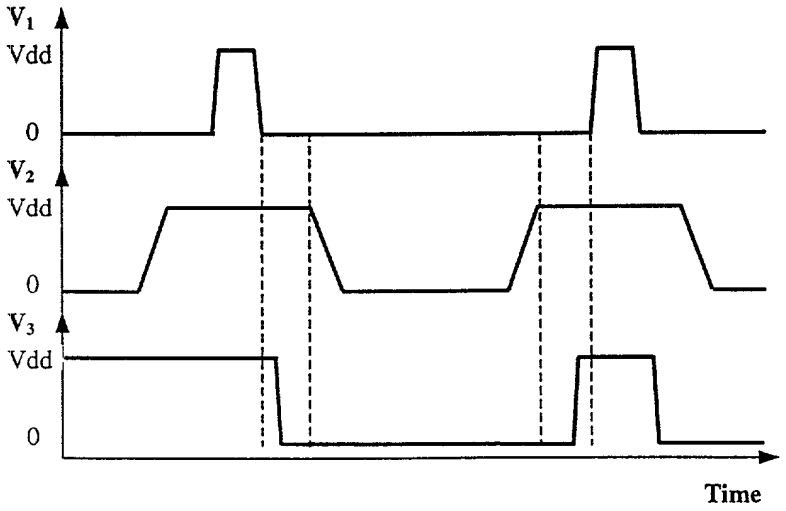
V_1
Vdd
0
V_2
Vdd
0
V_3
Vdd
0
Time

FIG. 5

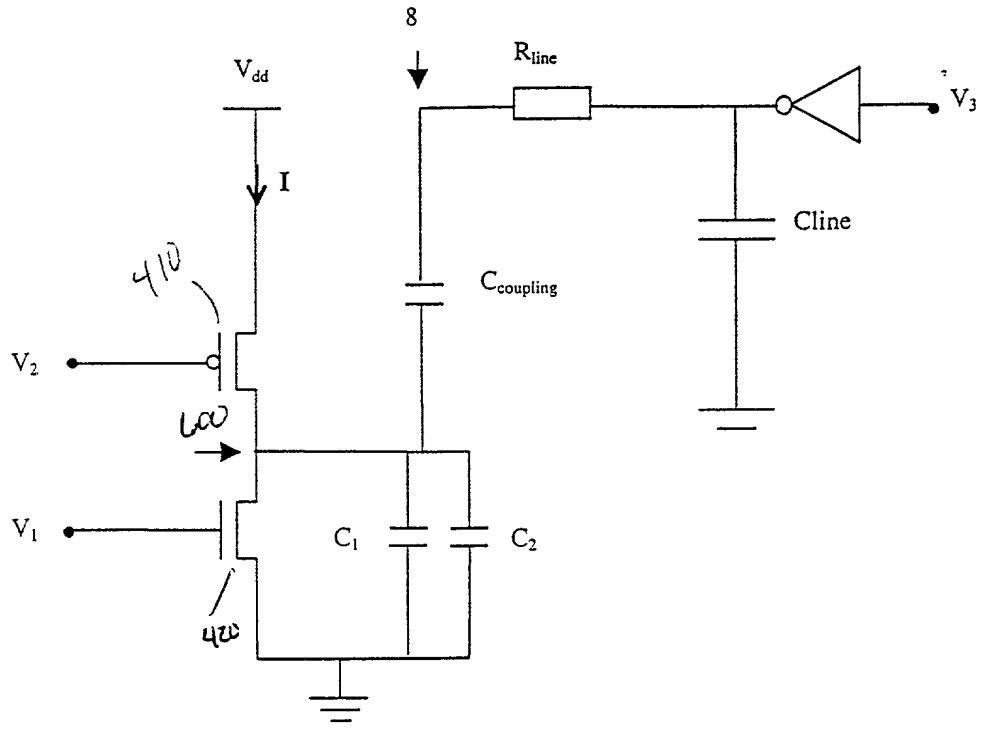

FIG. 4

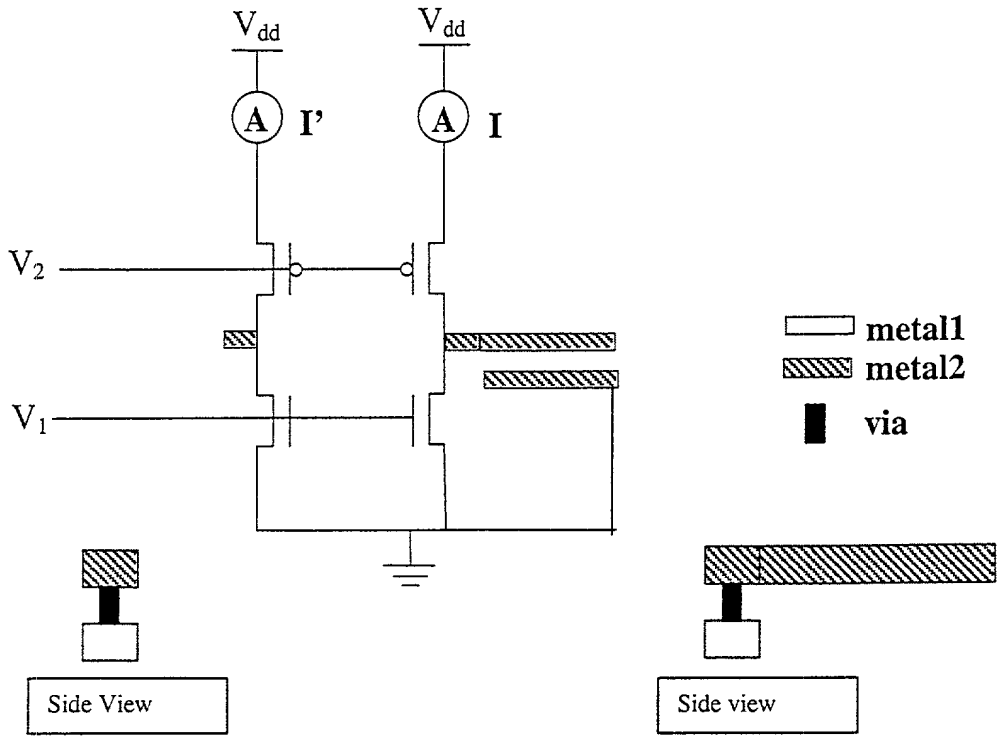

FIG. 7

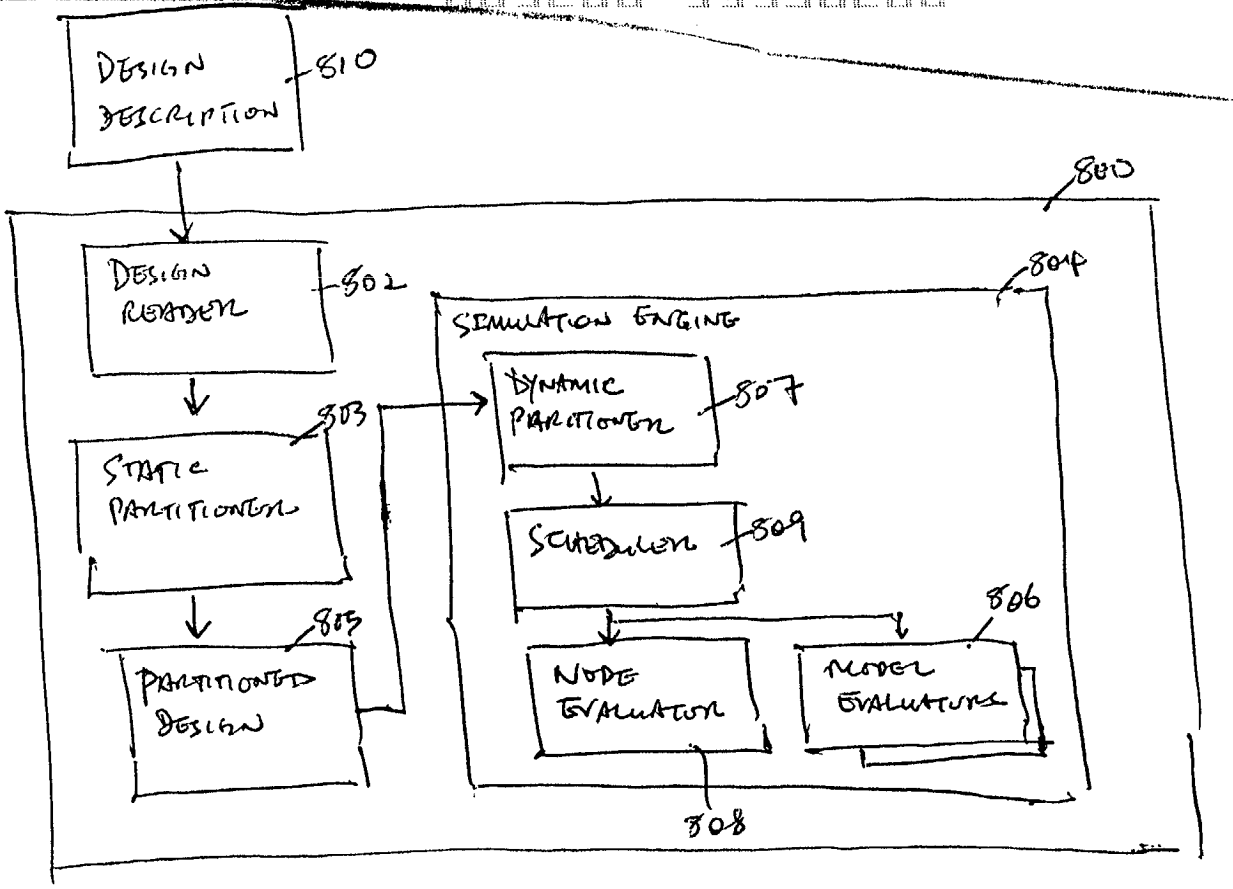
DESIGN DESCRIPTION
810
800
DESIGN READER
802
SIMULATION ENGINE
804
DYNAMIC PARTITIONER
807
STATIC PARTITIONER
803
SCHEDULER
809
PARTITIONED DESIGN
805
806
NODE EVALUATION
MODEL EVALUATORS
808

FIG. 8

PDB
916
900
902
API
PDB READ
904
PDB WRITE
908
PDB
APPLICATION UNIT
LOGICAL ORG.
PHYSICAL ORG.
906
910
912
914
PORT LAYOUT ANALYSIS APPLICATIONS
918

Figure 9

1000

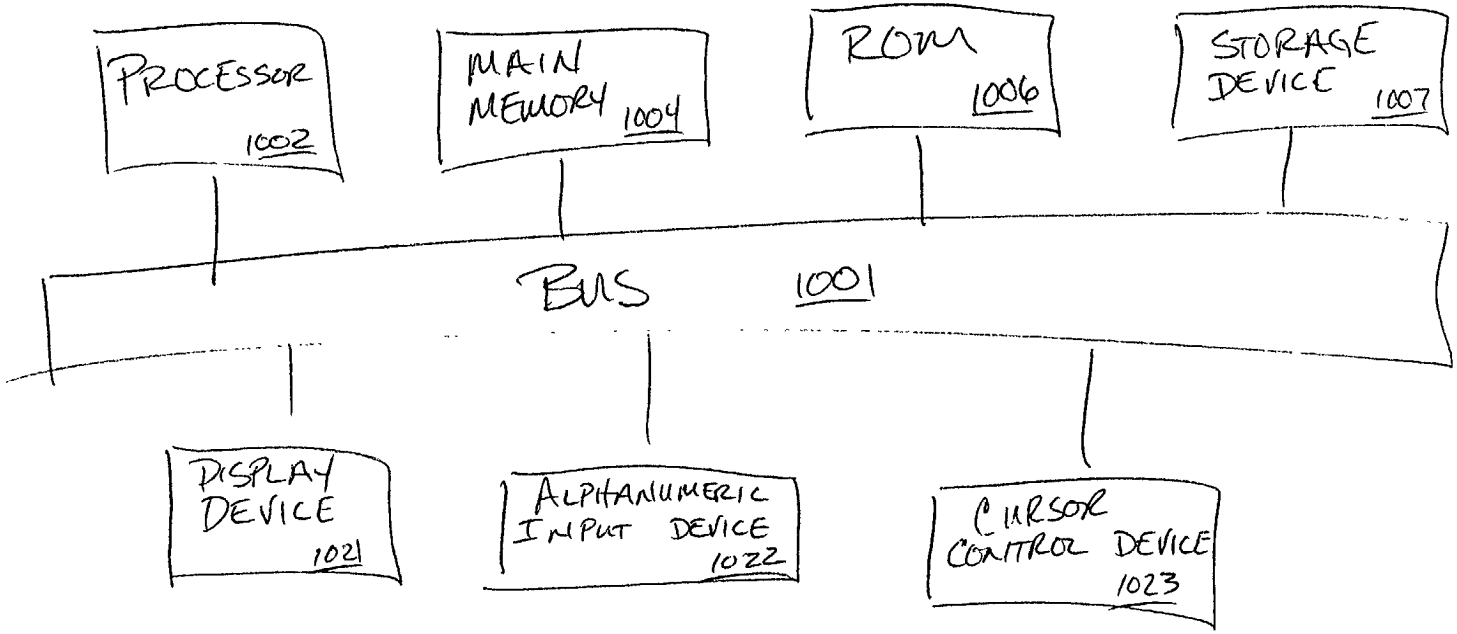
PROCESSOR
1002
MAIN MEMORY
1004
ROM
1006
STORAGE DEVICE
1007
BUS
1001
DISPLAY DEVICE
1021
ALPHANUMERIC INPUT DEVICE
1022
CURSOR CONTROL DEVICE
1023

FIG. 10

Attorney's Docket No.: 002282.P066 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CAPACITANCE MEASUREMENTS FOR AN INTEGRATED CIRCUIT

the specification of which

XX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Chun M. Ng, Reg. No. 36,878; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364;; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Paul Mendonsa (Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Paul Mendonsa (Name of Attorney or Agent), (503) 684-6200.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Roberto Suaya

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Second/Joint Inventor Sophie Gabillet

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____